

TCL_PLI, a Framework for Reusable, Run Time Configurable Test Benches

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ABSTRACT

10 A scripting approach to managing the test bench complexity issue is provided. Partitioning the functionality of a test bench between Verilog and a scripting language allows for a significant reduction in compile times during ASIC verification. If done correctly, partitioning also offers great potential for re-use of test bench components. The Tcl language was chosen as a basis for

15 implementing a library of PLI routines that allow fully customizable interpreters to be instantiated in Verilog test benches. This library allows multiple Tcl interpreters to be instantiated in a Verilog simulation. The Tcl interpreters can interact with the simulation and cause tasks to be executed in the Verilog simulation. It has been found the TCL_PLI library is extremely valuable in

20 speeding up verification efforts on multi-million gate ASICs.